IN THE CLAIMS:

1. (currently amended) A circuit providing protection against electrostatic discharge (ESD) for internal elements of an Integrated Circuit (IC), the circuit being connected to a power rail and a ground rail and to an inverter of a clamp preamplifier, said circuit comprises:

- a PMOSFET resistor with a gate connected to said ground rail, a drain connected to an ~~said inverter's~~ input node of said inverter, a source and a bulk connected to said power rail,
- an NMOSFET capacitor ~~with~~ having a gate connected to said ~~inverter's~~ input node of said inverter, a drain, a source and a bulk of said NMOSFET capacitor being connected to said ground rail, and
- a PMOSFET capacitor ~~with~~ having a gate connected to said ~~inverter's~~ input node of said inverter, a drain and a source of said PMOSFET capacitor being connected to said ground rail, and a bulk of said PMOSFET capacitor being connected to said power rail.

2. (currently amended) The circuit according to claim 1 wherein said NMOSFET capacitor has a non-linear capacitance characteristic.

3. (currently amended) The circuit according to claim 1 wherein said PMOSFET capacitor has a non-linear capacitance characteristic.

4. (currently amended) The circuit according to claim 1 wherein said NMOSFET capacitor and said PMOSFET capacitor have non-linear capacitance characteristics.

5. (Previously amended) The circuit according to any of the claim 1 wherein ratio of capacitance of said PMOSFET capacitor to capacitance of said NMOSFET capacitor decreases when voltage at said power rail exceeds NMOSFET threshold.

6. (currently amended) An integrated circuit comprising a circuit providing protection against an electrostatic discharge event, ~~according to any of claim 1.~~ the circuit providing protection being connected to a power rail and a ground rail and to an inverter of a clamp preamplifier, said circuit comprises:

- a PMOSFET resistor with a gate connected to said ground rail, a drain connected to an input node of said inventor, a source and a bulk connected to said power rail,
- an NMOSFET capacitor having a gate connected to said input node of said inverter, a drain, a source and a bulk of said NMOSFET capacitor being connected to said ground rail, and
- a PMOSFET capacitor having a gate connected to said input node of said inverter, a drain and a source of said PMOSFET capacitor being connected to said ground rail, and a bulk of said PMOSFET capacitor being connected to said power rail.